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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,810	03/18/2004	Shinichi Watanabe	250618US2	5884

22850 7590 05/04/2005

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/802,810	WATANABE, SHINICHI	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) *10 and 12-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 08/03/2004 is acceptable.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "a second insulating film including deuterium therein and formed on an inner surface of a trench which is formed in the semiconductor substrate; and an element isolation insulating layer formed in the trench and on the second insulating layer" of **claim 3, 12, and 19** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the

drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: gate insulating film **105** (page 5, line 7). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 10 and 12-17 are objected to because of the following informalities: each of these claims recites: "according to claim 8" but it is clear that the phrase should be "according to claim 9".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-2, 9-11, and 18** are rejected under 35 U.S.C. 102(b) as being anticipated by Rost et al. U.S. Patent 6,326,274 (the '274 reference).

Referring to **claims 1, 9-10, and 18**, the reference discloses a semiconductor device with an insulating layer including deuterium and an inherent method for manufacturing thereof comprising:

a semiconductor substrate ("substrate", Figs. 1-4);

a gate insulating film (no number) including deuterium therein (column 3, lines 20-67, particularly lines 28-32) and formed on the semiconductor substrate;

diffusion layers (not shown but must be present for the device to function) formed in the semiconductor substrate and located apart from each other to be adjacent to the gate insulating film;

a gate electrode (no number) formed on the gate insulating film;

a first insulating film including deuterium therein and formed on a side surface of the gate electrode (column 3, lines 38-40);

and a protective layer (ILD) formed so as to cover the first insulating film.

Note that although the reference does not explicitly call the ILD the protective layer, the ILD layer protects underlying elements from the (environmental) element therefore the ILD could be called a protective layer.

Referring to **claims 2 and 11**, the reference further discloses that the protective layer (ILD) is formed so as to cover the first insulating film and the gate insulating film (as is evident from the figures).

6. Claims 1-3, 5-6, 8-12, 14-15, 17-19, 21, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Kunikiyo U.S. Patent Application Publication 20020047169 (the '169 reference).

The '169 reference discloses in the figures, particularly Fig. 21, and respective portions of the specification a semiconductor device with an insulating layer including deuterium and an inherent method for manufacturing thereof as claimed.

Referring to **claims 1, 9-10, and 18**, the reference discloses a semiconductor device with an insulating layer including deuterium and an inherent method for manufacturing thereof comprising:

a semiconductor substrate (1/2 and the portion of the substrate above portion 1/2);

a gate insulating film (111/112) including deuterium therein (paragraph [0199]) and formed on the semiconductor substrate;

diffusion layers (4/6) formed in the semiconductor substrate and located apart from each other to be adjacent to the gate insulating film;

a gate electrode (13) formed on the gate insulating film;

a first insulating film (the portion of film 162 that is formed on a side surface of the gate) including deuterium therein and formed on a side surface of the gate electrode (paragraph [0230]);

and a protective layer (17) formed so as to cover the first insulating film.

Referring to **claims 2 and 11**, the reference further discloses that the protective layer (ILD) is formed so as to cover the first insulating film and the gate insulating film (as is evident from the figures).

Referring to **claims 3, 12, and 19**, the reference further discloses a second insulating film (58, Fig. 22, and note that STI 50 of Fig. 22 is the same as STI 3 of Fig. 21) including deuterium therein (paragraph [0281]) and formed on an inner surface of a trench (57) which is formed in the semiconductor substrate; and an element isolation insulating layer (61) formed in the trench and on the second insulating layer

Referring to **claims 5 and 14**, the reference further discloses that the protective layer (17) is one of an insulating layer including nitrogen ("silicon nitride", paragraph [0212]), meeting the limitation of the claimed Markush group of "one of an insulating layer including nitrogen and an oxide aluminum layer".

Referring to **claims 6, 15, and 21**, the reference further discloses that a third insulating film (such as 18 or the top portion of film 162) is formed on the gate electrode.

Referring to **claims 8, 17, and 23**, the reference further discloses that the first insulating film (162) extends on the one of the diffusion layers.

Claim Rejections - 35 USC § 102

7. **Claims 1,2,4-11,13-18 and 20-23** are rejected under 35 U.S.C. 102(e) as anticipated by Parekh et al. U.S. Patent Application Publication 20050032314 (the '314 reference) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Parekh et al. in view of Kunikiyo U.S. Patent Application Publication 20020047169 (the '169 reference).

The '314 reference discloses a semiconductor device with an insulating layer including deuterium and an inherent method for manufacturing thereof as claimed or substantially as claimed.

Specifically, with reference to **claims 1, 9-10, and 18**, the reference discloses in Fig. 12 and respective portions of the specification a semiconductor device with an insulating layer including deuterium and an inherent method for manufacturing thereof comprising:

a semiconductor substrate (702);

a gate insulating film (709) formed on the semiconductor substrate;

diffusion layers (706.x, x=1, 2) formed in the semiconductor substrate and located apart from each other to be adjacent to the gate insulating film;

a gate electrode (712) formed on the gate insulating film;

a first insulating film (710) including deuterium therein and formed on a side surface of the gate electrode (paragraph [0056], and "on a side surface of the gate electrode" is interpreted broadly, i.e., the first insulating film does not have to be in contact with the side surface of the gate electrode, as in, for example, "On side surfaces of the gate electrode 104, sidewalls 109 are formed with first and second offset films 107 and 108 interposed therebetween", of U.S. Patent Application Publication 20020137297 by Kunikiyo, Fig. 28, paragraph [0008] or as in "The semiconductor device with an insulating layer including deuterium according to claim 1, further

comprising a side wall insulating film formed around the side surface of the gate electrode" of claim 7 of the present invention, which means that either (or both) of the first insulating film or the side wall insulating film is not in contact with the side surface of the gate electrode);

and a protective layer (720) formed so as to cover the first insulating film.

However, the reference fails to explicitly disclose that the gate insulating film (709) includes deuterium therein. Nevertheless, the '314 reference discloses, also in paragraph [0056] that "the presence of deuterium in alumina layer 710 may passivate defects in gate dielectrics 709 and STI structures 707.1 and 707.2". In other words, it appears that the reference teaches that deuterium from alumina layer 710, in an annealing process, penetrates into the gate insulating film ("gate dielectric") to correct defects in the gate insulating film, or in other words, appears to teach that the gate insulating film (709) includes deuterium therein.

In the alternative, let's assume that the deuterium from alumina layer 710, in an annealing process, does not penetrate into the gate insulating film to correct defects in the gate insulating film as disclosed by the '314 reference. The '169 reference, in also disclosing a semiconductor device with an insulating layer including deuterium and an inherent method for manufacturing thereof as detailed above, teaches in paragraph [0058] that "gate insulating film...contains deuterium atoms....enhances the reliability of the MOSFET", thereby teaching that gate insulating film includes deuterium therein enhances the reliability of the device including the gate. Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '314 reference's gate insulating film 709 such that the gate insulating film includes deuterium therein. One would have been motivated to make such a

change because gate insulating film including deuterium therein enhances the reliability of the device including the gate and the gate insulating film.

Referring to **claims 2 and 11**, the '314 reference or the '314 reference in view of the '169 reference further discloses that the protective layer (720) is formed so as to cover the first insulating film (710) and the gate insulating film (as is evident from the figures).

Referring to **claims 4, 13, and 20**, the '314 reference or the '314 reference in view of the '169 reference further discloses a capacitor (not shown) electrically connected to one of the diffusion layers (paragraph [0039], the '314 reference).

Referring to **claims 5 and 14**, the '314 reference or the '314 reference in view of the '169 reference further discloses that the protective layer (720) is one of an insulating layer including nitrogen ("silicon nitride", paragraph [0043]), meeting the limitation of the claimed Markush group of "one of an insulating layer including nitrogen and an oxide aluminum layer".

Referring to **claims 6, 15, and 21**, the '314 reference or the '314 reference in view of the '169 reference further discloses that a third insulating film (such as capping dielectric 716 or the top portion of film 710 or film 720) is formed on the gate electrode.

Referring to **claims 7, 16, and 22**, the '314 reference or the '314 reference in view of the '169 reference further discloses a side wall insulating film (718) formed around the side surface of the gate electrode.

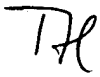
Referring to **claims 8, 17, and 23**, the '314 reference or the '314 reference in view of the '169 reference further discloses that the first insulating film (710) extends (at least, or at least in an intermediate step) on the one of the diffusion layers.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tu-Tu Ho
April 30, 2005